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Docket No.: W&B-INF-860

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : UDO HARTMANN

Filed : Concurrently herewith

Title : CIRCUIT AND METHOD FOR TESTING A DATA MEMORY

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent 6,195,771 B1 (Tanabe et al.), dated February 27, 2001;

European Patent Application EP 0 828 257 A2 (Tanabe et al.), dated March 11, 1998;

Tadahiko Sugibayashi et al.: "A Distributive Serial Multi-Bit Parallel Test Scheme for Large Capacity DRAMs", IEICE Trans. Electron., Vol. E77-C, No. 8, August 1994, pp. 1323-1327;

Respectfully submitted,

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